

REMARKS

Claims 1-8 are pending in the present application. Claims 1-3 have been amended. Claims 4-8 have been presented herewith.

Priority Under 35 U.S.C. 119

Applicant notes the Examiner's acknowledgment of the Claim for Priority under 35 U.S.C. 119, and receipt of the certified copy of the priority document.

Drawings

Enclosed are two (2) red-inked drawing Annotated Sheets, wherein Figs. 2 and 3 have been denoted as "PRIOR ART", as required. Also enclosed are two (2) drawing Replacement Sheets, incorporating the above noted corrections. **The Examiner is respectfully requested to acknowledge receipt and acceptance of the drawing Replacement Sheets.**

Claim Rejections-35 U.S.C. 103

Claims 1-3 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Nakamura et al. reference (Japanese Patent Publication No. 7-249973) in view of the Kimura et al. reference (U.S. Patent No. 5,016,223). This rejection is respectfully traversed for the following reasons.

The interface circuit of claim 1 includes in combination among other features a 3-

state buffer "which is driven by a second power voltage that is supplied from the power unit of said second apparatus and in which an output of a signal that is supplied from said second apparatus is controlled by an electric potential at said power node".

Applicant respectfully submits that these features would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together for at least the following reasons.

The Examiner has primarily relied upon Fig. 1 of the Nakamura et al. reference, interpreting circuit 1 as the first apparatus of claim 1 with power source 3 as its corresponding power unit, circuit 2 as the second apparatus of claim 1 with power source 4 as its corresponding power unit, the point at which power source 3 is connected to circuit 1 as the power node of claim 1, and buffer 6 as the 3-state buffer of claim 1.

However, as described in paragraph [0018] of the Nakamura et al. reference as relied upon, sag detector 50 in Fig. 1 detects a level of supply voltage output from power source 4, and generates a detection output indicative thereof. As further described in paragraph [0021] of the Nakamura et al. reference, buffer 6 as shown in Fig. 1 provides the output of circuit 1 and is controlled by the detection output from sag detector 50. Accordingly, buffer 6 in Fig. 1 of the Nakamura et al. reference is not driven by a second power voltage that is supplied from a power unit (power source 4) of a second apparatus (circuit 2), as would be necessary to meet the features of claim 1. Moreover, since the detection signal as output from sag detector 50 in Fig. 1 of the

Nakamura et al. reference controls buffer 6, buffer 6 is not controlled by an electric potential at a power node (point at which power source 3 is connected to circuit 1), as would be necessary to meet the further features of claim 1. Also, buffer 6 does not provide as an output a signal supplied from a second apparatus (circuit 2), as would be necessary to meet the still further features of claim 1. The secondary Kimura et al. reference as relied upon does not overcome these above noted deficiencies of the Nakamura et al. reference. Applicant therefore respectfully submits that the interface circuit of claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claim 1 is improper for at least these reasons.

With further regard to this rejection, the interface circuit of claim 1 also includes in combination among other features an analog switch “which is driven by said second power voltage and in which a connection between an output side of said 3-state buffer and a logic circuit in said first apparatus is controlled by the electric potential at said power mode”.

The Examiner has acknowledged that the Nakamura et al. reference does not disclose an analog switch as featured in claim 1. In an effort to overcome this acknowledged deficiency of the Nakamura et al. reference, the Examiner has relied upon Fig. 5(a) of the Kimura et al. reference as disclosing 3-state buffers 34 and 35, and analog switch 30. The Examiner has alleged that it would have been obvious at the time of the invention to have included the analog switch of the Kimura et al.

reference in Fig. 1 system of the Nakamura et al. reference. The Examiner has alleged that the “suggestion or motivation for doing so would have been to provide an analog switch, which depending upon a received signal control its operation it turns on/off preventing/allowing power/signal to flow”. Applicant respectfully disagrees for the following reasons.

As described on page 11 of the present application, since analog switch 30 in Fig. 1 is on/off controlled on the basis of the electric potential at power node NP, when power node NP becomes equal to ground voltage, analog switch 30 is turned off. Thus, the output signal of 3-state buffer 13c does not appear at the output side of analog switch 30. Therefore, the electric potential at the power node NP is held at ground voltage, and interface 13 is perfectly turned off. As a result, when the power source of ROM writing apparatus 10A is turned off in a state where the power source of user board 2 is turned on, wraparound of the power source of user board 2 is blocked and heat generation or thermal breakdown of interface 13 is consequently prevented.

Applicant respectfully submits that the Examiner has not established necessary and sufficient motivation to modify the circuit in Fig. 1 of the Nakamura et al. reference in view of the Kimura et al. reference. The Examiner’s suggested motivation to modify the circuit of the Nakamura et al. reference to include an analog switch such as shown in the Kimura et al. reference appears to be based merely upon impermissible hindsight. That is, the Examiner has merely asserted that the suggestion or motivation to modify the primary reference to include an analog switch would be that “for doing so

would have been to provide an analog switch". The Examiner has identified no specific teaching as drawn from the Kimura et al. reference as a reason to modify the circuit of the Nakamura et al. reference as suggested. In absence of such specifically relied upon teaching in the Kimura et al. reference, it would appear that the Examiner has randomly picked elements of the circuit of the Kimura et al. reference and in hindsight has incorporated the hand picked elements into the circuit of the Nakamura et al. reference. For instance, it is not clear from the Kimura et al. reference why it would be necessary or desirous to control a connection between an output side of a 3-state buffer and a logic circuit in a first apparatus.

Moreover, even if motivation existed for modifying the circuit of the Nakamura et al. reference in view of the Kimura et al. reference (which motivation Applicant does not admit exists), there would be no reason to provide an analog switch in the Fig. 1 circuit of the Nakamura et al. reference specifically driven by a second power voltage from a power unit (power source 4) of a second apparatus (circuit 2), as would be necessary to meet the features of claim 1. Also, there would be no motivation to provide an analog switch as specifically controlled by the electric potential at a power node (the point at which power source 3 is connected to circuit 1), as would be necessary to meet the still further features of claim 1. Applicant therefore respectfully submits that the interface circuit of claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claim 1 is improper for at least these additional reasons.

Applicant respectfully submits that the interface circuit of claim 2 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together for at least somewhat similar reasons as set forth above with respect to claim 1. Particularly, the prior art as relied upon does not disclose or suggest a 3-state buffer driven by a second power voltage supplied from a power unit (power source 4) of a second apparatus (circuit 2) such as in the Nakamura et al. reference, as would be necessary to meet the features of claim 2.

Applicant also respectfully submits that the Examiner has not established necessary and sufficient motivation for modifying the circuit in Fig. 1 of the Nakamura et al. reference in view of the Kimura et al. reference, for at least somewhat similar reasons as set forth above with respect to claim 1. The motivation as suggested by the Examiner is merely that for doing so would have been to provide an analog switch. Moreover, even if proper motivation existed for modifying the Nakamura et al. reference as suggested (which motivation Applicant does not admit exists), there would be no motivation to provide an analog switch in the Nakamura et al. reference specifically driven by a second power voltage from a second apparatus, and so that the analog switch is controlled by a signal output from a voltage detector, as would be necessary to meet the further features of claim 2. Applicant therefore respectfully submits that the interface circuit of claim 2 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, for at least these reasons.

Applicant respectfully submits that the interface circuit of claim 3 would not have

been obvious in view of the prior art as relied upon by the Examiner for at least somewhat similar reasons as set forth above. The prior art as combined would not disclose or suggest a 3-state buffer driven by a second power voltage supplied from a power unit of a second apparatus, whereby the 3-state buffer is controlled in accordance with a control voltage provided from an analog switch, as featured in claim 3. The Examiner has not provided sufficient and necessary motivation to modify the circuit of the Nakamura et al. reference in view of the Kimura et al. reference. Moreover, even if proper motivation existed for modifying the primarily relied upon Nakamura et al. reference (which motivation Applicant does not admit exists), there would be no motivation to provide the analog switch as specifically driven by a second power voltage, and to provide the output of the analog switch as a control voltage to a 3-state buffer, as would be necessary to meet the features of claim 3. Applicant therefore respectfully submits that the interface circuit of claim 3 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claim 3 is improper for at least these reasons.

Claims 4-8

The interface circuit of claim 4 includes in combination a first circuit; a second circuit; a 3-state buffer “that sends data from the second circuit to the first circuit”; a protective diode “connected in a reverse direction between a data input terminal of the first circuit and a power output terminal of the first power unit, that protects the first

circuit, wherein the 3-state buffer has a driving terminal that receives the power voltage from the second circuit as a driving voltage, and a control terminal that receives the power voltage from the first circuit as a control voltage”; and an analog switch “that prevents current produced by a potential difference between the driving voltage and the control voltage from flowing to the protective diode, by cutting off sending of the data from a data output terminal of the 3-state buffer to the data input terminal of the first circuit when supply of the power voltage from the first power unit is terminated”.

As noted above, the Examiner has primarily relied upon Fig. 1 of the Nakamura et al. reference. However, buffer 6 in Fig. 1 of the Nakamura et al. reference does not receive a power voltage from a second circuit (circuit 2) as a driving voltage, and does not receive a power voltage from a first circuit as a control voltage. Moreover, there would be no reason to provide an analog switch in the Fig. 1 circuit of the Nakamura et al. reference to specifically control voltage in view of the Kimura et al. reference, as would be necessary to meet the further features of claim 4. Particularly, Fig. 5(a) of the Kimura et al. reference as specifically relied upon merely discloses in general 3-state buffers 34 and 35, and analog switch 30. There is no specific teaching in the Kimura et al. reference that would suggest using analog switch 30 to cut off sending of data when supply of power voltage from a first power unit is terminated, to prevent current from flowing to a protective diode. In absence of such specific motivation, such a rejection as based upon the prior art as relied upon by the Examiner would be based merely on impermissible hindsight. Applicant therefore respectfully submits that claims 4-8

distinguish over and would not have been obvious in view of the prior art as relied upon by the Examiner for at least these reasons.

Conclusion

Applicant respectfully submits that the amendments to claims 1-3 are merely for the purpose of improving readability and form, not to further distinguish over the relied upon prior art. Accordingly, the amendments to claims 1-3 should not be construed as narrowing scope within the meaning of *Festo*.

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

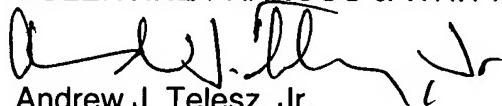
Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of two (2) months to October 25, 2006, for the period in which to file a response to the outstanding Office Action. The required fee of \$450.00 should be charged to Deposit Account No. 50-0238.

Serial No. 10/720,387
OKI.598
Amendment dated October 24, 2006

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

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Enclosures: Two (2) drawing Annotated Sheets
Two (2) drawing Replacement Sheets

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ANNOTATED SHEET

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Fig. 2 PROOF APPARATUS

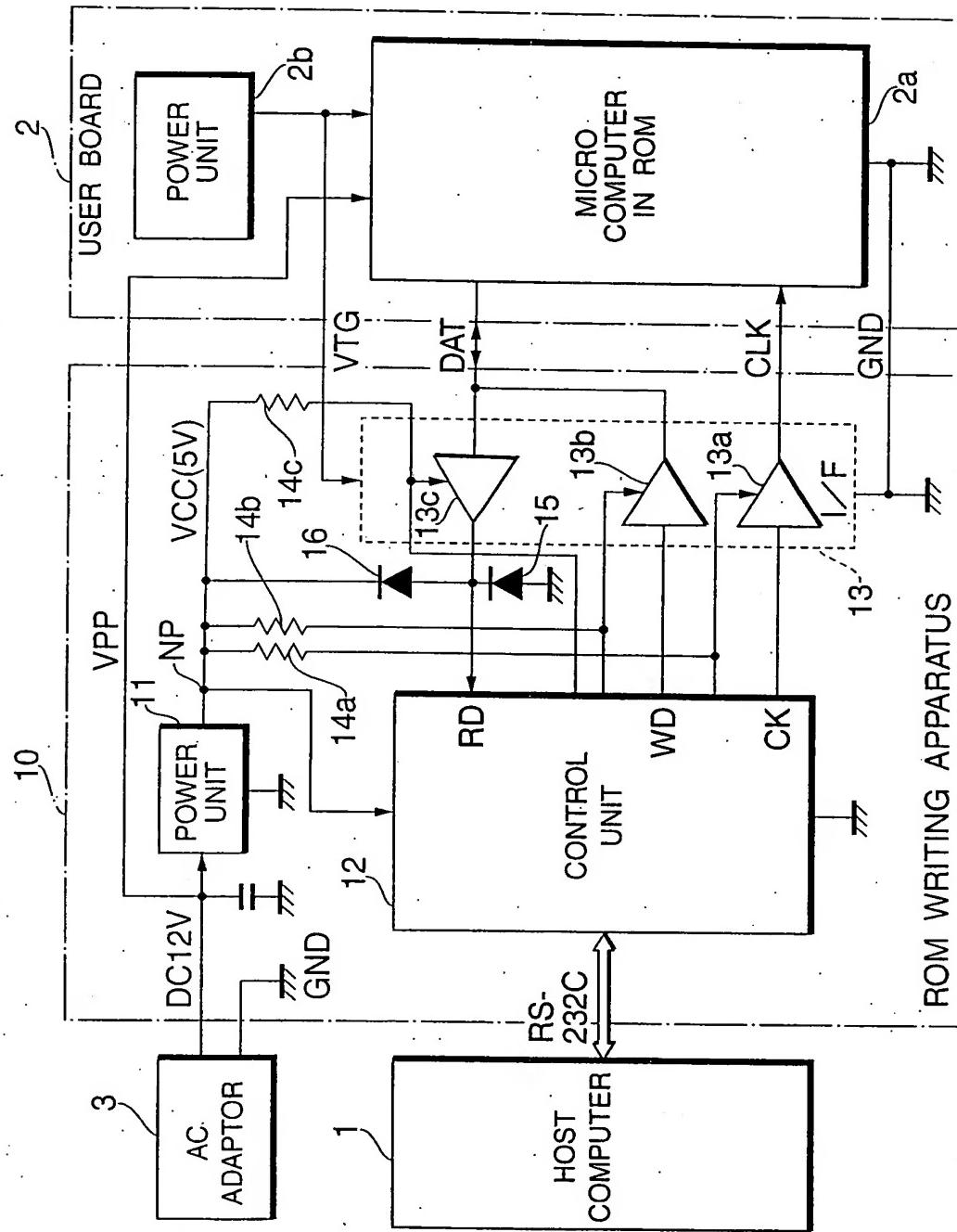


Fig.3 PRIOR ART

